

MSI MS-7364 Ver:10

CPU:

Intel Prescott LGA775 -Mainstream CPU

System Chipset:

North Bridge : VIA P4M900/P4M890

South Bridge : VIA VT8237A/VT8237S

On Board Chipset:

LPC Super I/O -- W83627EHG

LAN(PHY) --- Realtek 8201CL

Ausio HD Codec -- Realtek ALC 888/883/655

BIOS --SPI+LPC FLASH ROM

CLOCK Chip :

CLOCK Generator -- ICS9LPR704AGLF

Main Memory:

DDRII * 1 +DDR I * 1

Expansion Slots:

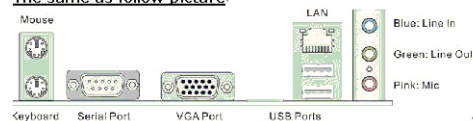
PCI SLOT * 1

PWM:

VRM11 ST L6703 3Phase

Rear I/O:

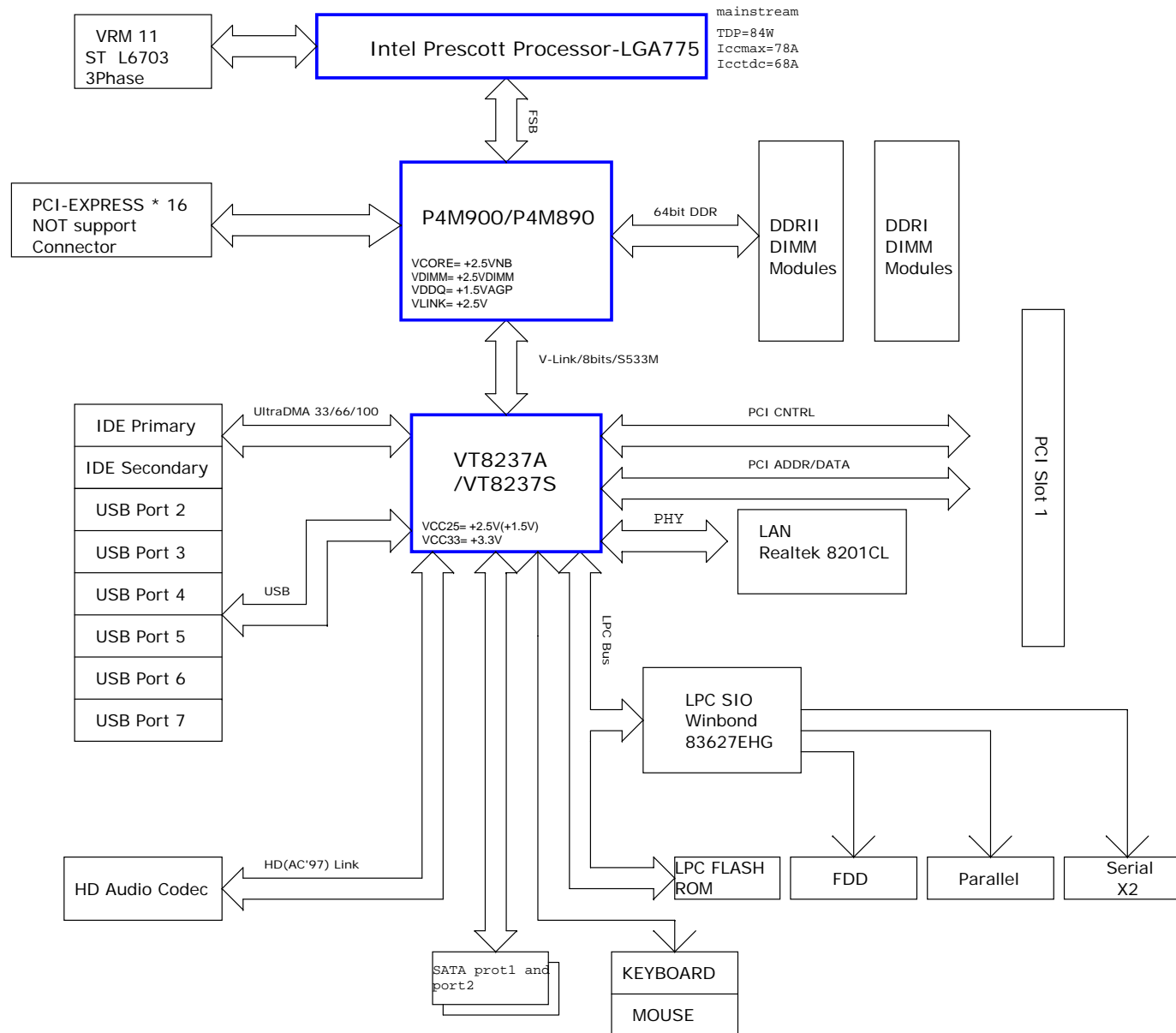
The same as follow picture:



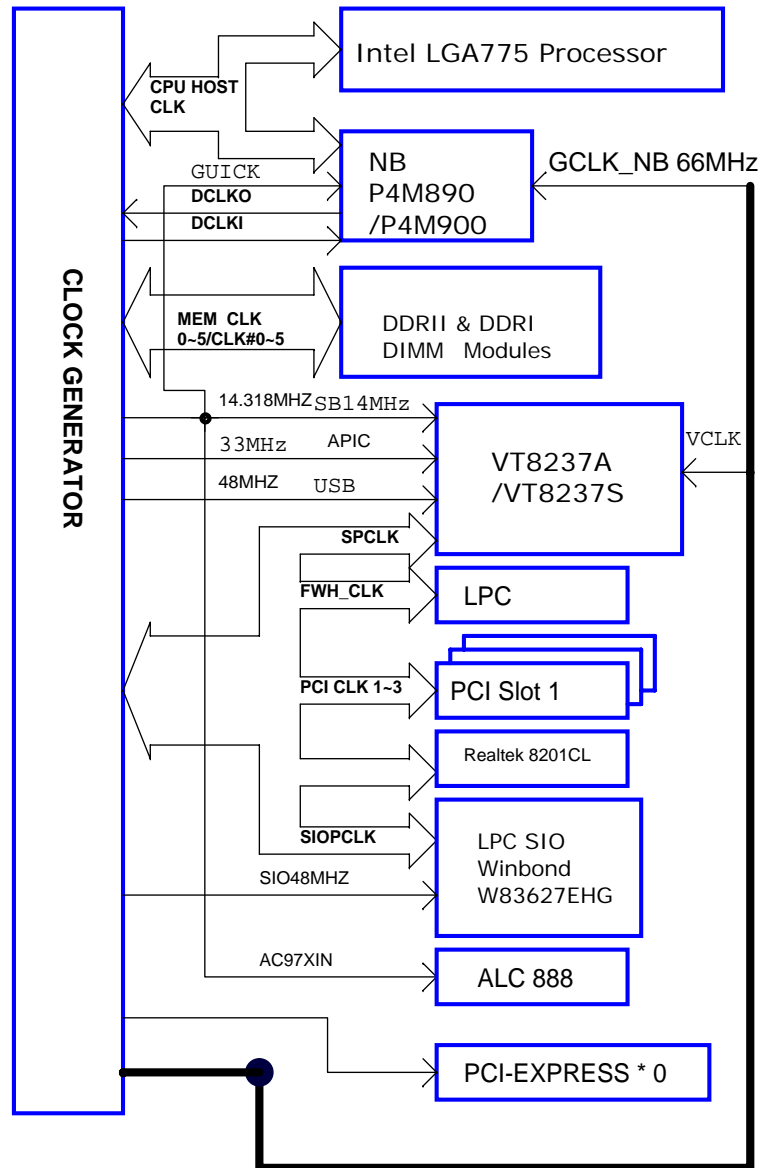
CHIPSET P4M900/P4M890 + VT8237A/VT8237S

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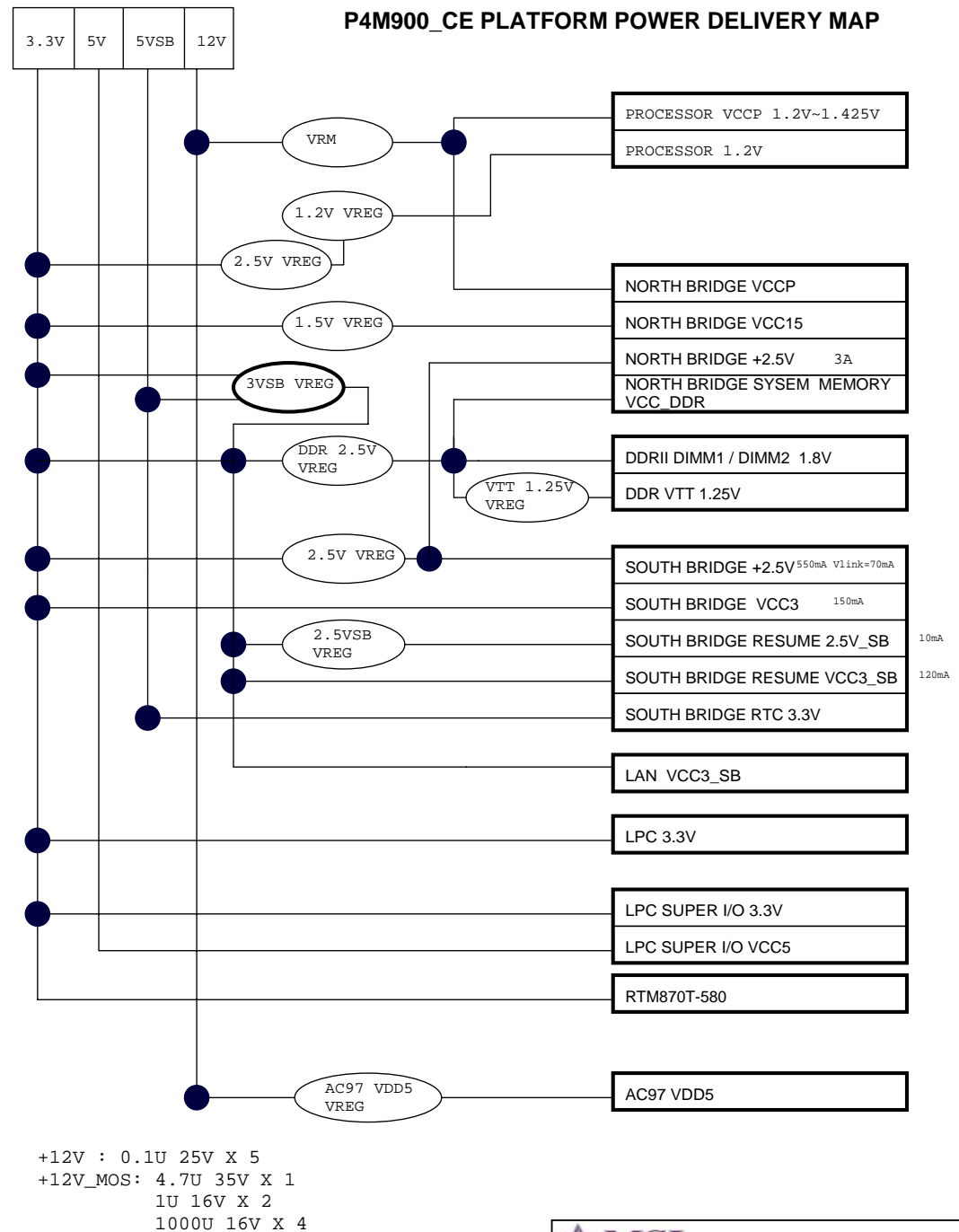
Block Diagram



**P4M890/P4M900
PLATFORM CLOCK GENERATOR MAP
CHIPSET P4M890/P4M900 + VT8237A/VT8237S**



P4M900_CE PLATFORM POWER DELIVERY MAP



+12V : 0.1U 25V X 5
+12V_MOS: 4.7U 35V X 1
1U 16V X 2
1000U 16V X 4

VT8237R_PLUS GPIO Function Define

PIN NAME	Default Function	Function define
GPO0 (VDDS)	GPO0	4.7K ohm Pull up to VCC3_SB
GPO1(VDDS)	GPO1	4.7K ohm Pull up to VCC3_SB
GPO2/SUSA# (VDDS)	SUSA#	4.7K ohm Pull up to VCC3_SB
GPO3/SUSST#(VDDS)	SUSST#	4.7K ohm Pull up to VCC3_SB
GPO4/SUSCLK(VDDS)	SUSCLK	4.7K ohm Pull up to VCC3_SB
GPO5/CPUSTP#	CPUSTP#	4.7K ohm Pull up to VCC3
GPO6/PCISTP#	PCISTP#	4.7K ohm Pull up to VCC3
GPO7/GNT5	GPO7	8.2K ohm Pull up to VCC3
GPO8/GPI8/VGATE	GPO8	2.7K ohm Pull up to VCC3
GPO9/UDPWREN	UDPWREN	NC
GPO10/GPI10/PICD0	GPO10	1K ohm Pull up to VCC3
GPO11/GPI11/PICD1	GPO11	1K ohm Pull up to VCC3
GPO12/GPI12/INTE#	GPO12	8.2K ohm Pull up to VCC3
GPO13/GPI13/INTF#	GPO13	8.2K ohm Pull up to VCC3
GPO14/GPI14/INTG#	GPO14	8.2K ohm Pull up to VCC3
GPO15/GPI15/INTH#	GPO15	8.2K ohm Pull up to VCC3
GPO20/GPI20/ACSDIN2/PSC0#	GPI20/ACSDIN2	4.7K ohm Pull down
GPO21/GPI21/ACSDIN3/PSC1#/SLPBTN#	GPI21/ACSDIN3	4.7K ohm Pull down
GPO22/GPI22/GHI#	GPI22	4.7K ohm Pull up to VCC3
GPO23/GPI23/DPSLP	GPI23	4.7K ohm Pull up to VCC3
GPO24/GPI24 /GPIOA	GPIOA	2.2K ohm Pull up to VCC3 SEL Vlink Manual mode
GPO25/GPI25 /GPIOB	GPIOB	2.2K ohm Pull down SEL IOQ Depth=8 Level
GPO26/GPI26/SMBDT2 (VDDS)	SMBDT2	2.7K ohm Pull up to VCC3_SB
GPO27/GPI27/SMBCK2 (VDDS)	SMBCK2	2.7K ohm Pull up to VCC3_SB
GPO28/GPI28/VIDSEL	GPO28 /VIDSEL	SATA_LED
GPO29/GPI29/VRDSLP	GPO29 /VRDSLP	4.7K ohm Pull down
GPO30/GPI30 /GPIOC	GPIOC	2.2K ohm Pull up to VCC3 SEL Host Clock=Auto mode
GPO31/GPI31 /GPIOD	GPIOD	2.2K ohm Pull down SEL GTL pull up=Enable

PIN NAME	Default Function	Function define
GPI0 (VBAT)	GPI0	1M ohm Pull up to VBAT
GPI1 (VSUS3)	GPI1	ATADET0=>Detect IDE1 ATA100/66
GPI2/EXTSMI# (VSUS3)	EXTSMI#	4.7K ohm Pull up to VCC3_SB
GPI3/RING# (VSUS3)	RING#	RING# 4.7K ohm Pull up to VCC3_SB
GPI4/LID# (VSUS3)	LID#	ATADET1=>Detect IDE2 ATA100/66
GPI5/BATLOW# (VDDS)	BATLOW#	4.7K ohm Pull up to VCC3_SB
GPI6/AGPBZ	AGPBZ	4.7K ohm Pull up to VCC3
GPI7/REQ5	GPI7	8.2K ohm Pull up to VCC3
GPI9/UDPWREN	UDPWR	10K ohm Pull down
GPI16/INTRUDER# (VBAT)	INTRUDER#	1M ohm Pull up to VBAT
GPI17/CPUMISS	CPUMISS	4.7K ohm Pull up to VCC3_SB
GPI18/AOLGP1/THRM#	THERM#	4.7K ohm Pull up to VCC3_SB
GPI19/APICLK	APICLK	APICLK

USB	Port	DATA +/-	OC#
Rear	LAN_USB1	USB2- USB2+ USB3- USB3+	OC#1 (OC#0~3)
Front	JUSB2	USB4- USB4+ USB6- USB6+	OC#4 (OC#4~7)
	JUSB1	USB5- USB5+ USB7- USB7+	

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 DDR11	1010000B	DCLKA0/MDCLKA#0 DCLKA1/MDCLKA#1 DCLKA2/MDCLKA#2
DIMM 2 DDR1	1010000B	DCLKA0/MDCLKA#0 DCLKA1/MDCLKA#1 DCLKA2/MDCLKA#2

PCI RESET DEVICE

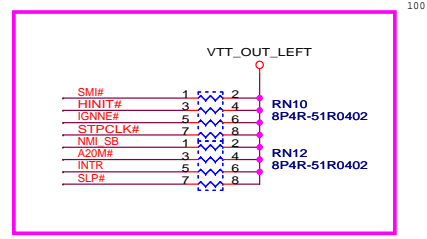
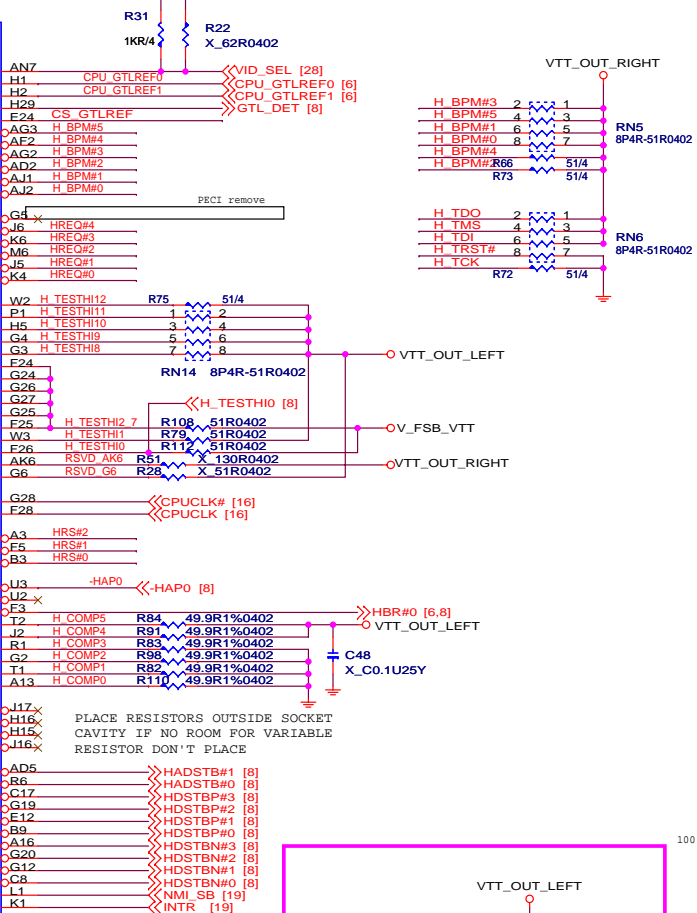
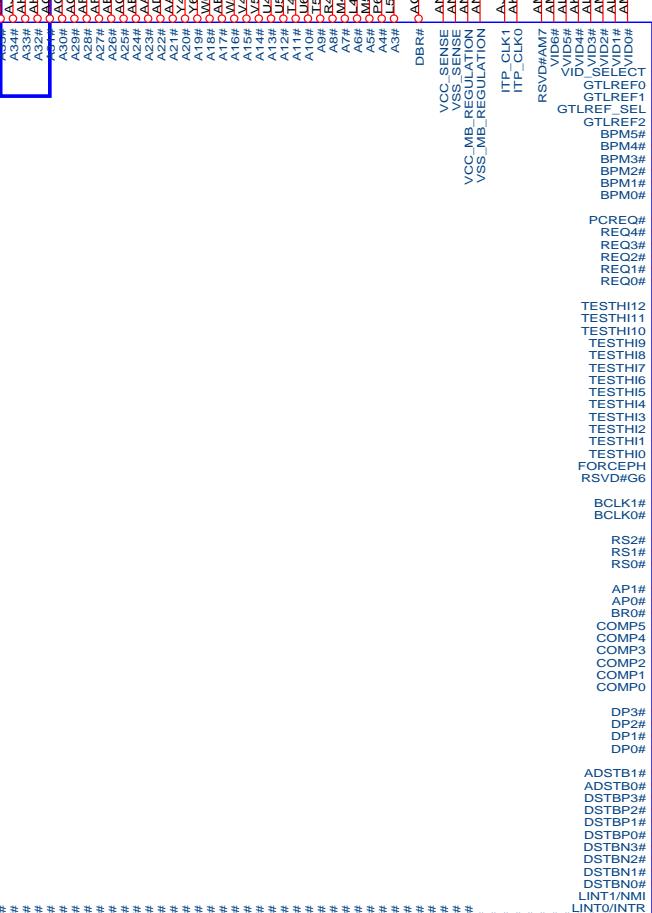
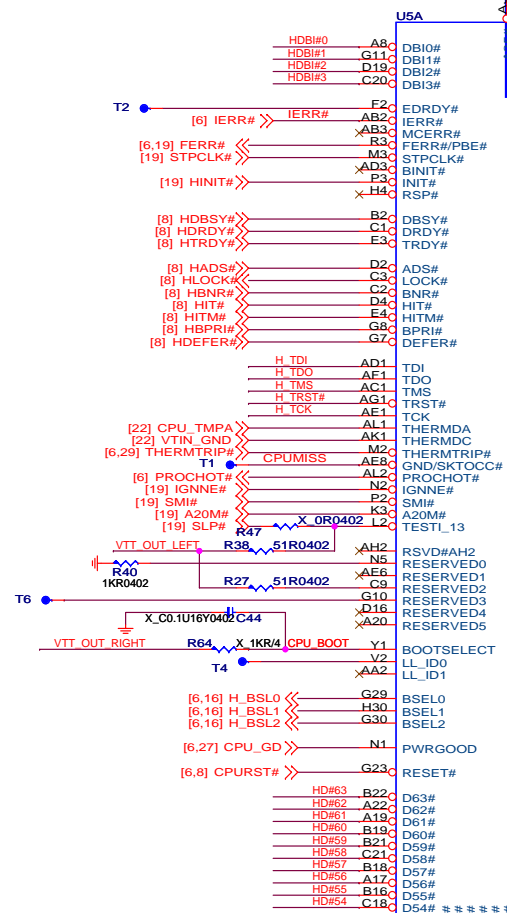
Signals	Target
PCIRST#1	PCI slot 1 , NB
PCIRST#2	Super I/O
PCIRST#3	FWH
HD_RST#	Primary IDE

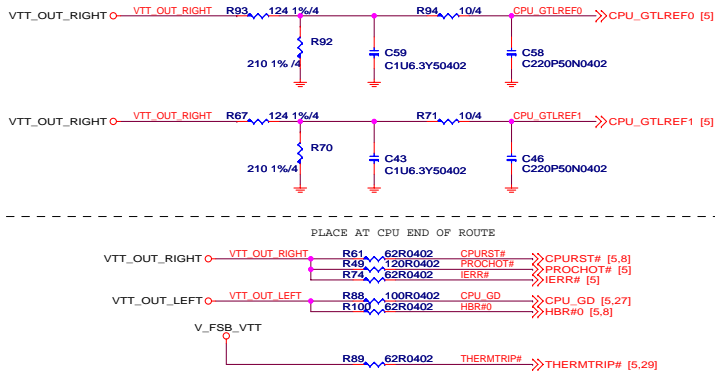
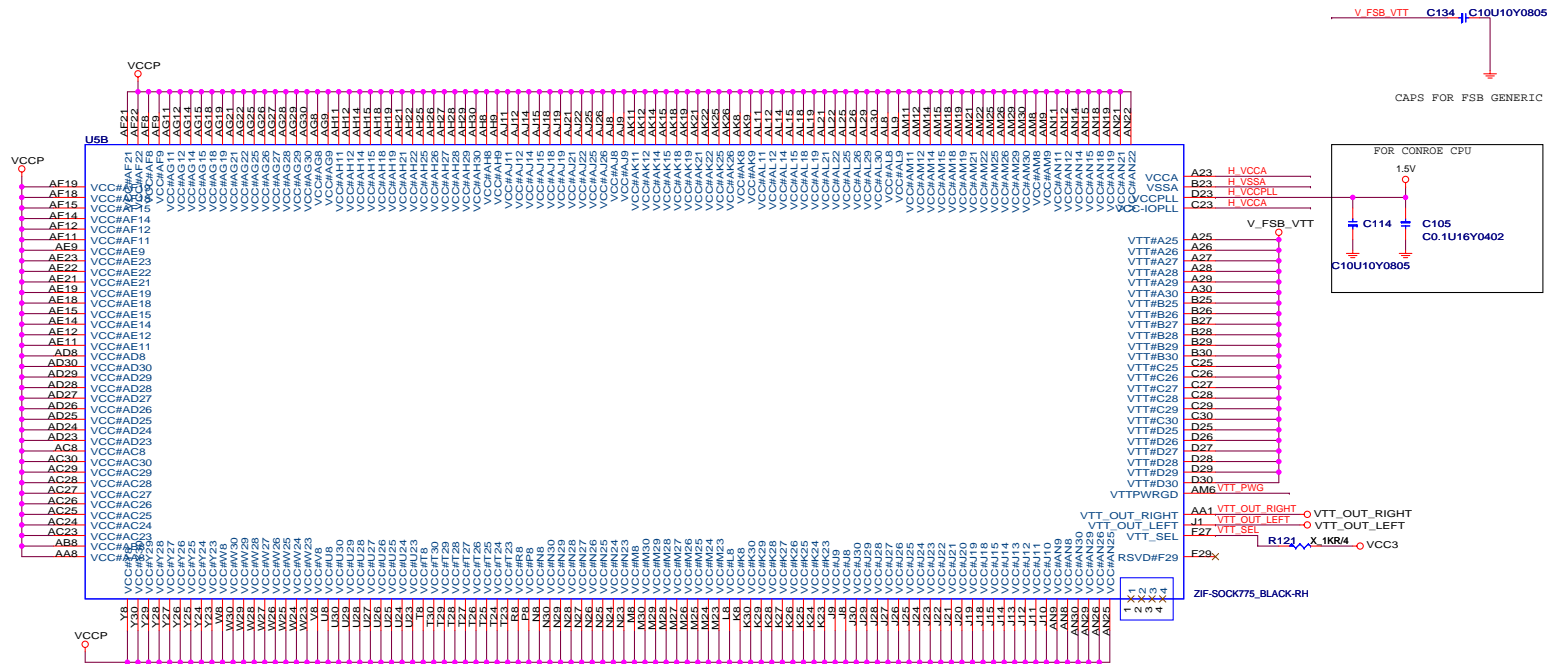
PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PCIREQ#1 PCIGNT#1	AD20	PCI_CLK2	PIN : 2

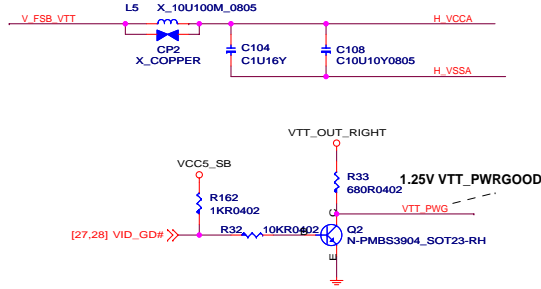
[8] HDBI#[0..3] << HDBI#[0..3]
[8] HA#[3..33] << HA#[3..33]
[28] VID[0..7] << VID[0..7]
[8] HREQ#[0..4] << HREQ#[0..4]
[8] HD#[0..63] << HD#[0..63]
[8] HRS#[0..2] << HRS#[0..2]

CPU SIGNAL BLOCK

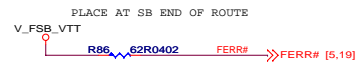
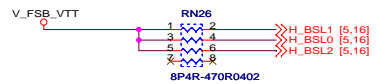


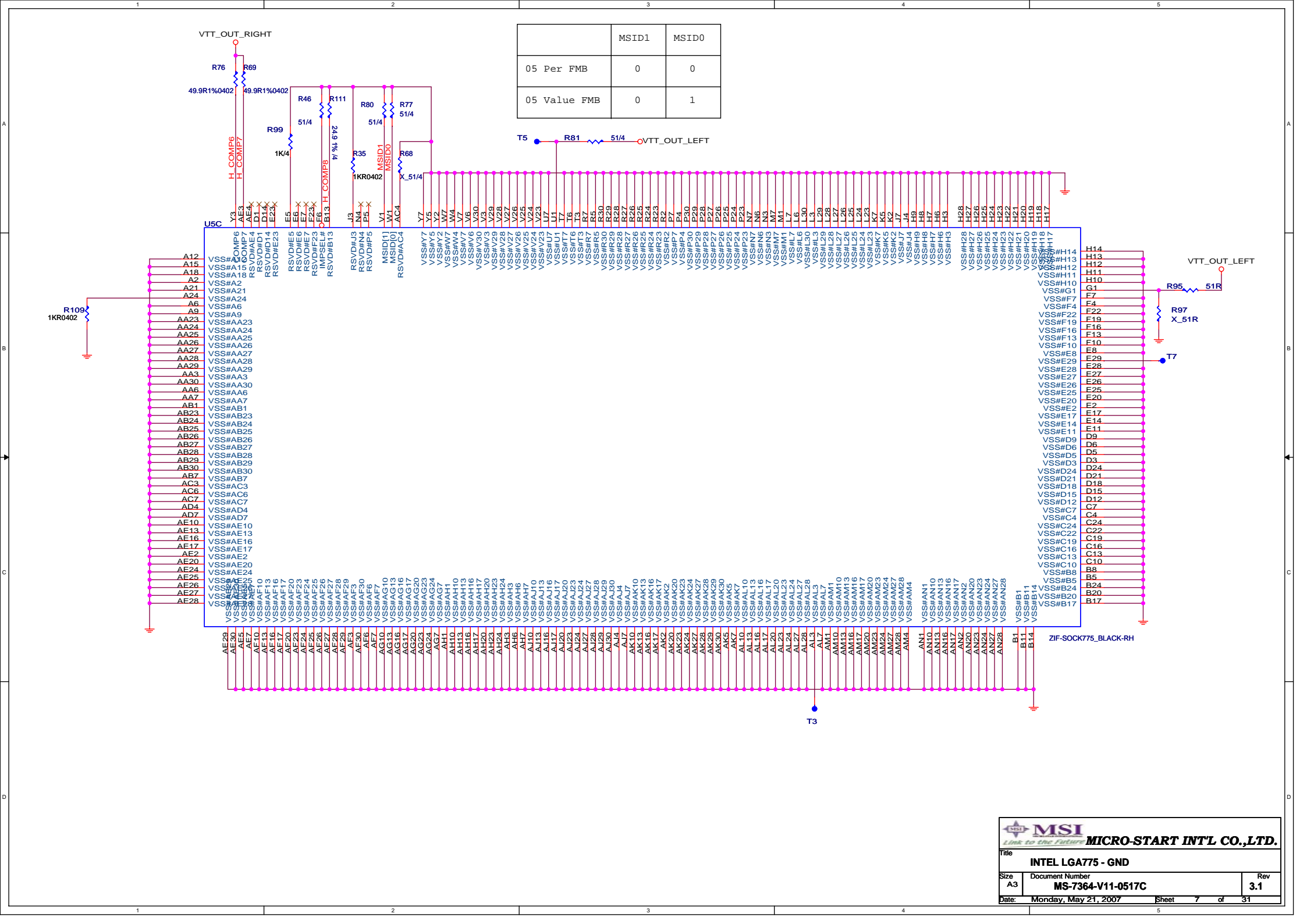


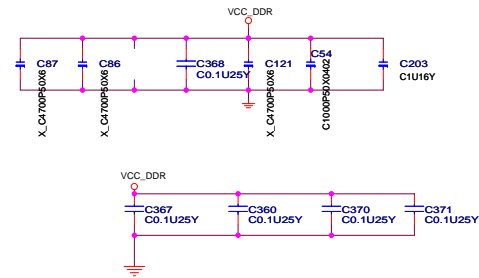
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS



FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS
AND CEDAR MILL ARE SUPPORTED





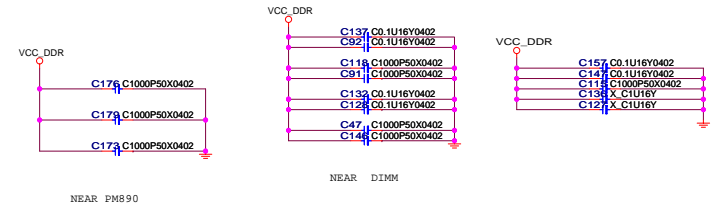
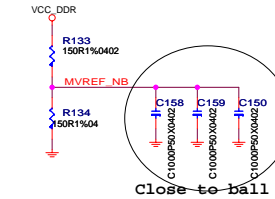


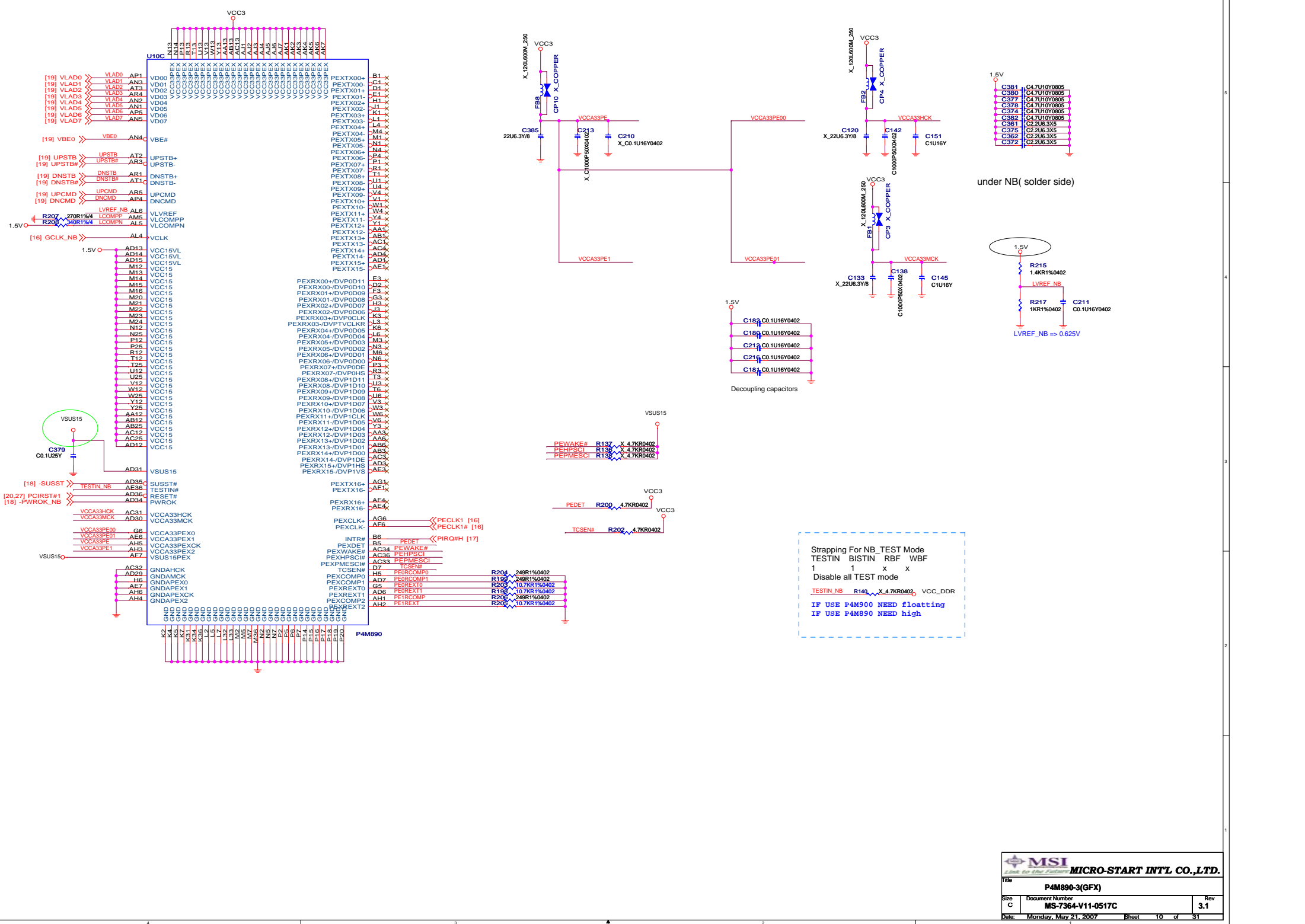
CLOSE TO DIMM

Test Point
(Place near their respective balls of NB)

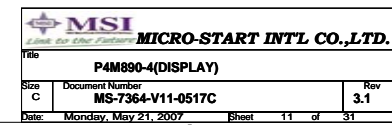
NOTE: DQS/DQS# => OTHER:W:S:W:OTHER=15:10:5:10:15

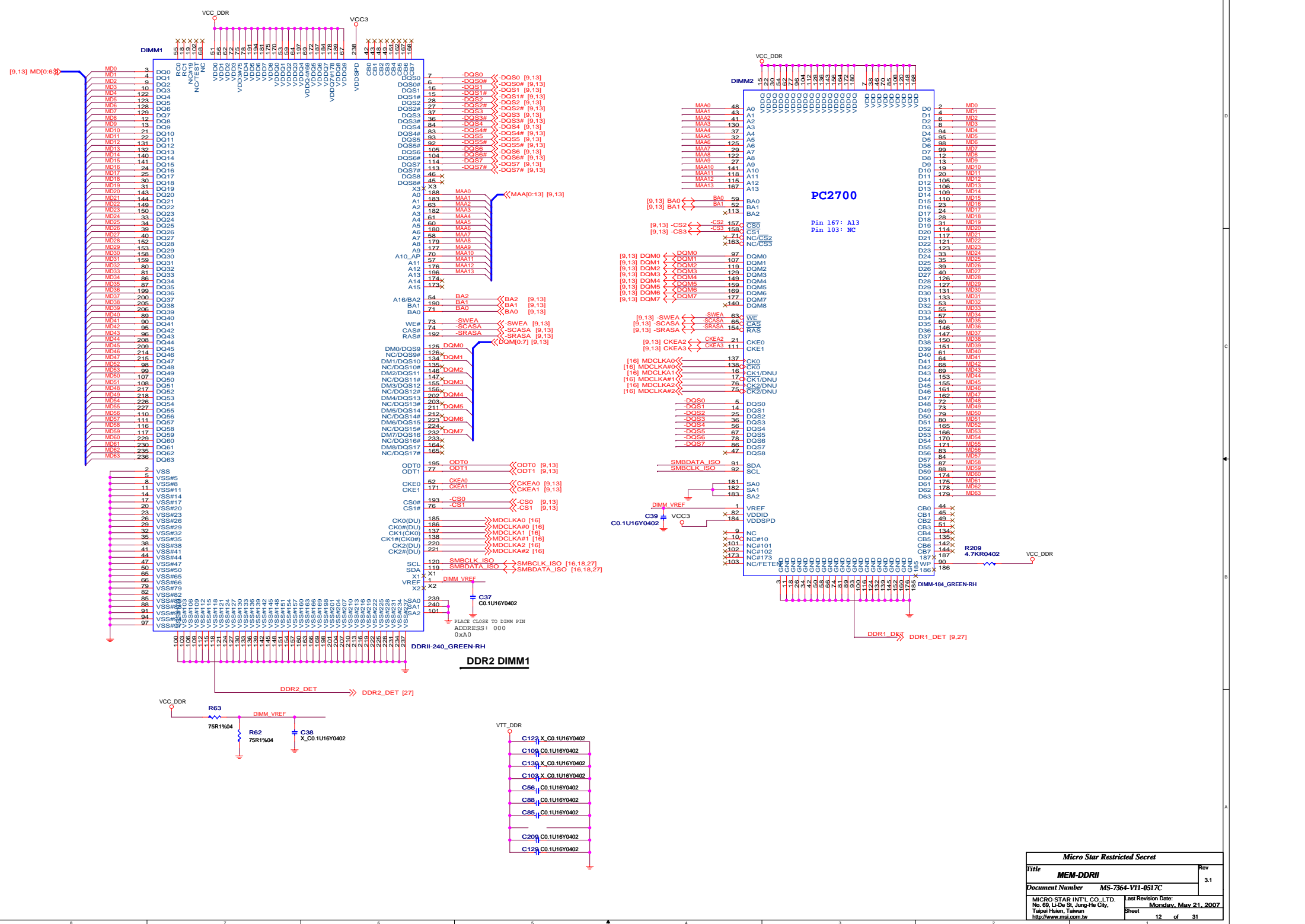
```
MCLKO+/- as short as passable
MCLKIT = DCLKx + 2 "
```





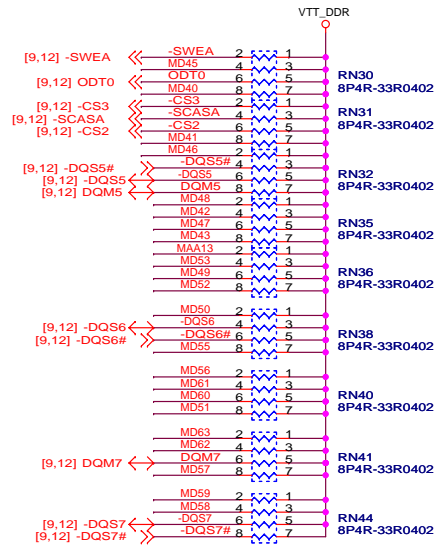
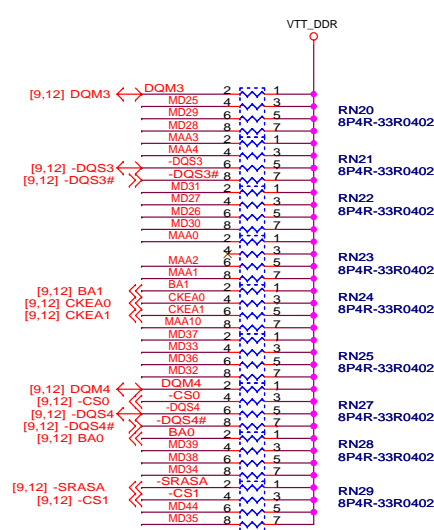
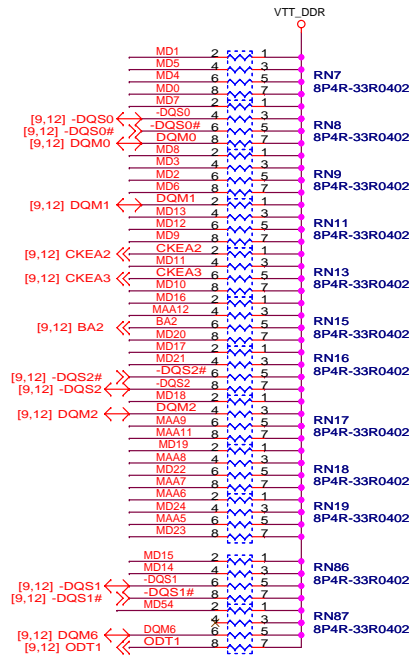
Strapping For NB_TEST Mode
TESTIN BISTN RBF WBF
1 1 x x
Disable all TEST mode
TESTIN NB R140 X 4.7KR0402 VCC_DDR
IF USE P4M900 NEED floating
IF USE P4M890 NEED high



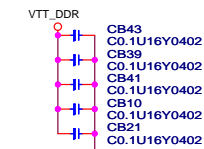
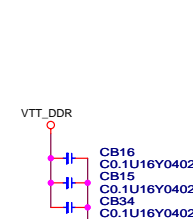
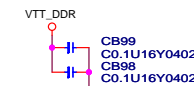
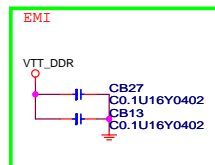
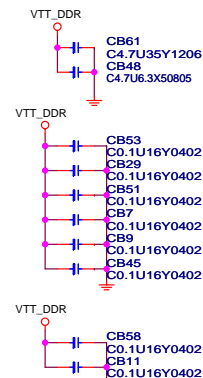
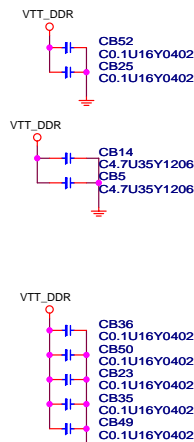
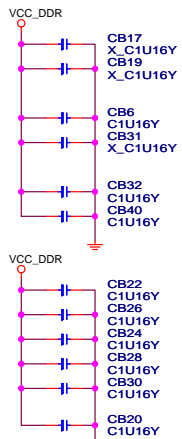
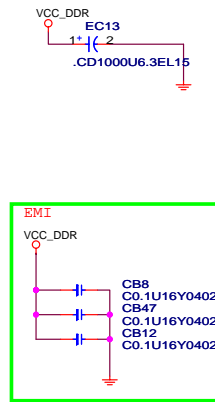


DIMM1 & 2 Terminations

[9,12] MAA[0:13] << MAA[0:13] [9,12] MD[0:63] << MD[0:63]

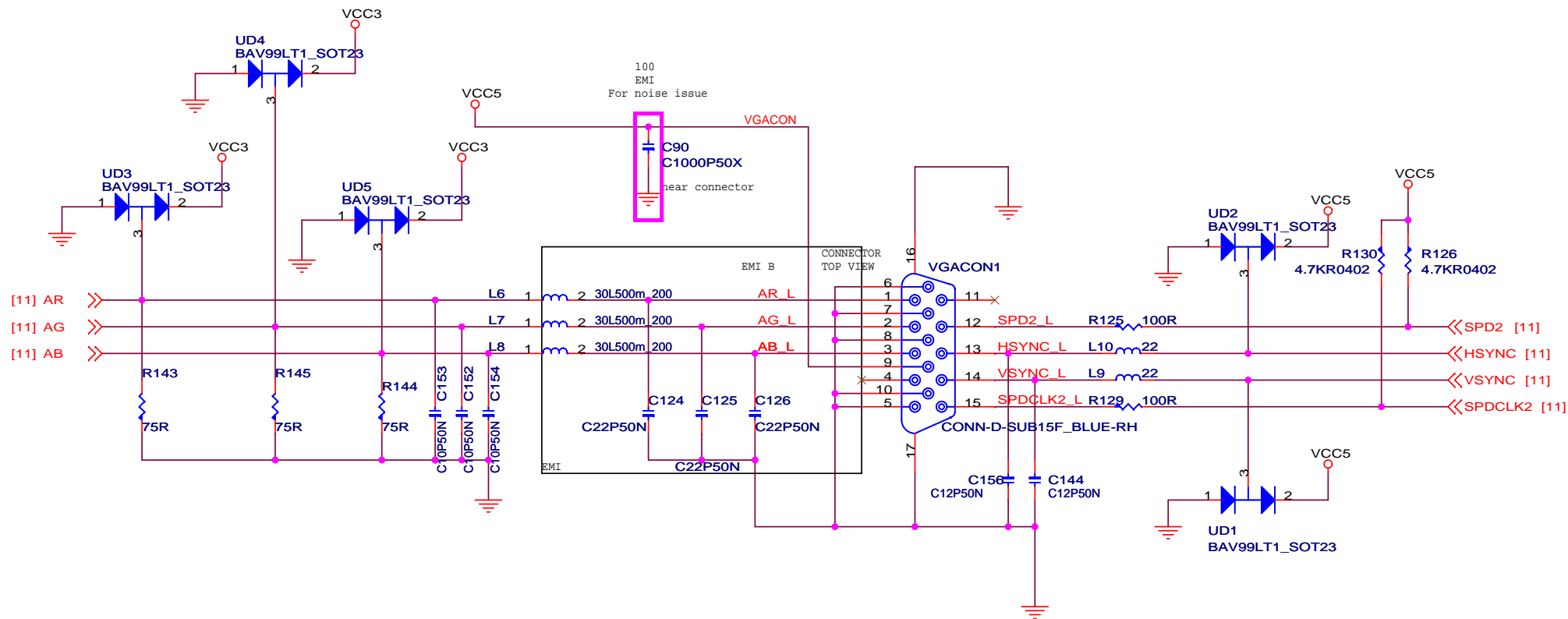



V_SM_VTT DECOUPLING CAPS

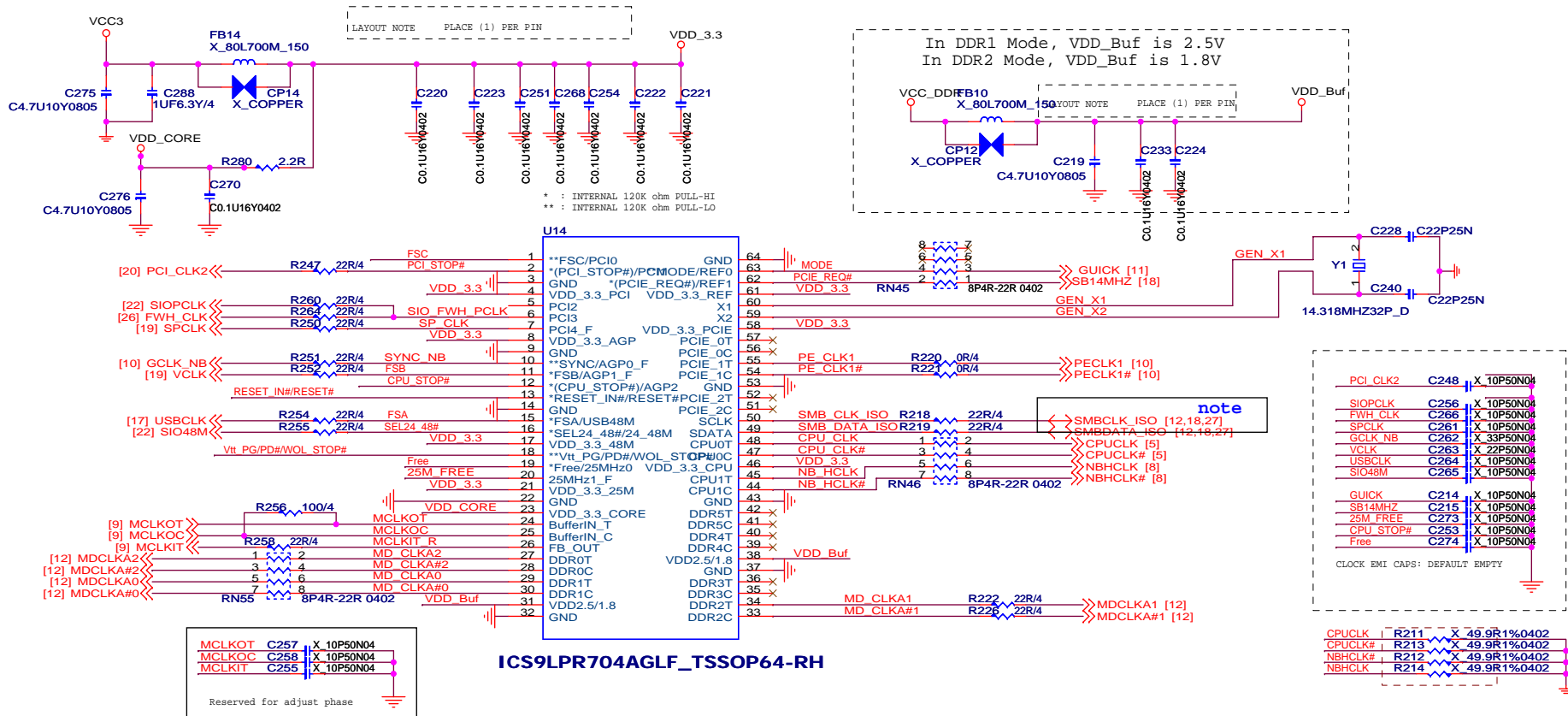


12V ==> 5.5A for x16 slot ,75 Watt
3.3V==> 3A
3.3Vaux==>375mA

VGA CONNECTOR



 MSI <small>Micro-Start International, Ltd.</small> <i>Link to the Future</i>		MICRO-START INT'L CO.,LTD.	
Title			
VGA Connector			
Size	Document Number		Rev
Custom	MS-7364-V11-0517C		3.1
Date:	Monday, May 21, 2007	Sheet	15 of 31



	1 (Pull High)	0 (Pull Low)
SYNC	PCIEX clocks are synchronous with CPU.	PCIEX clocks are asynchronous with CPU.
SEL24_48#	Pin16 = 24MHz	Pin16 = 48MHz
MODE	Notebook mode	Desktop mode
Free	25Mhz-0 is free running	25Mhz-0 is stoppable

Intel P4(775) Table

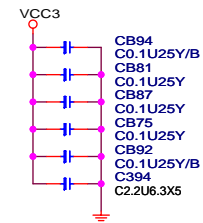
FS4	FS3	FS2	H_BSL1	H_BSL0	CPU
0	0	0	0	0	266
			0	1	133
			1	0	200
			1	1	166

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title Clock Generator RTM870T-580

Size Custom Document Number MS-7364-V11-0517C Rev 3.1

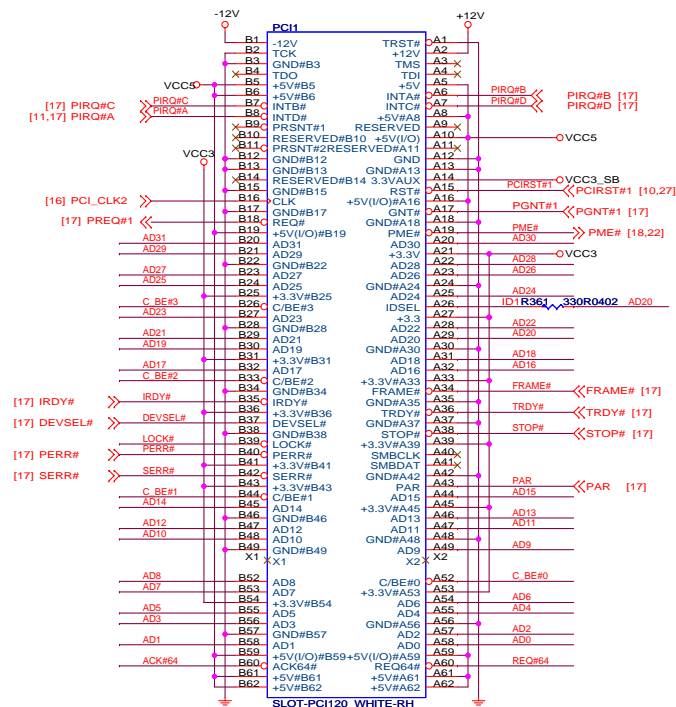
Date: Monday, May 21, 2007 Sheet 16 of 31



If use VT8237A R227=6.04K
If use VT8237S R227=5.62K

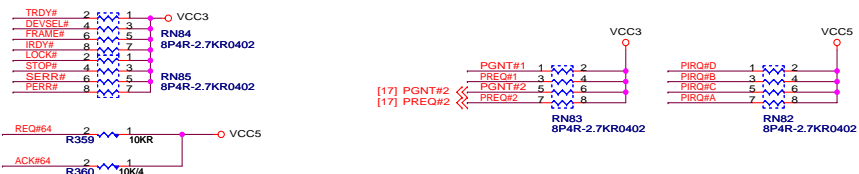
[17] AD[0..31] >> AD[0..31]
[17] C_BE#[0..3] >> C_BE#[0..3]

PCI SLOT 2

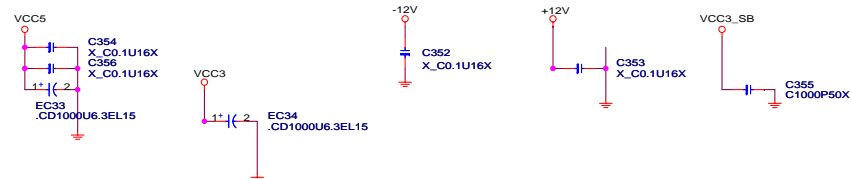


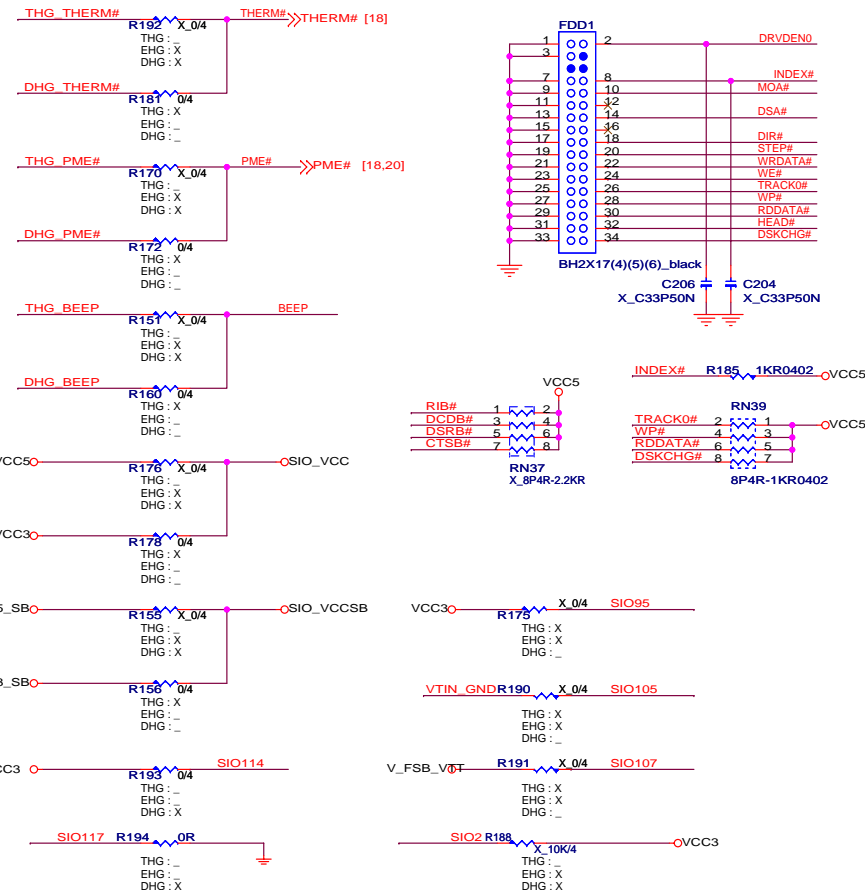
IDSEL = AD20
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



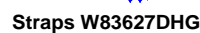


RTSA#	L: CFAD=2E *	H: CFAD=4E
SOUTB	L: 24MHz	H: 48MHz
SOUTA	L: KBC DISABLE *	H: KBC ENABLE
DTRA#	L: nnp i/o default addr *	H: clear nnp i/o addr

RTSA#	L: CFAD=2E *	H: CFAD=4E
SOUTA	L: KBC DISABLE *	H: KBC ENABLE
DTRA#	L: DISAB E Logical Device	H: ENAB E Logical Devi

RTSA#	L: CFAD=2E *	H: CFAD=4E
GP50	L: TTL LEVEL	H: VRM10 LEVEL
SOUTA	L: KBC DISABLE *	H: KBC ENABLE
DTA#	L: DISABLE SPI *	H: ENABLE SPI

issue

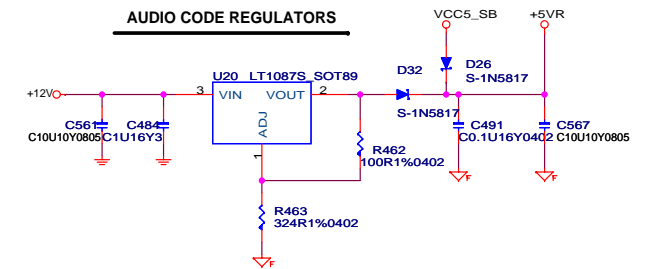
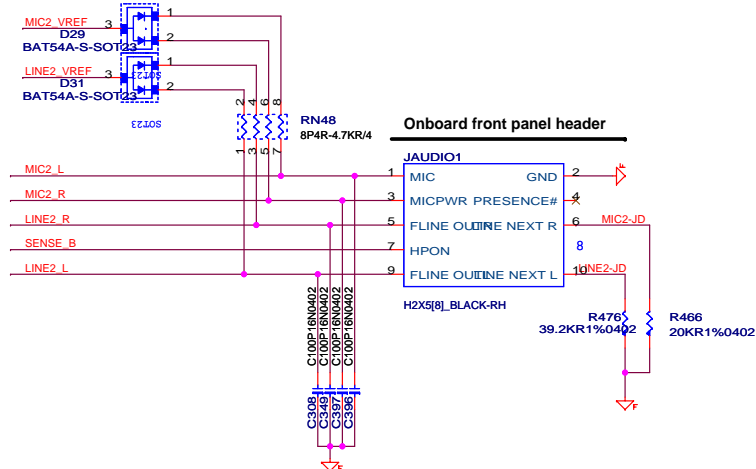
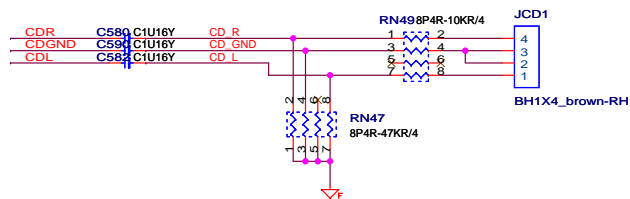
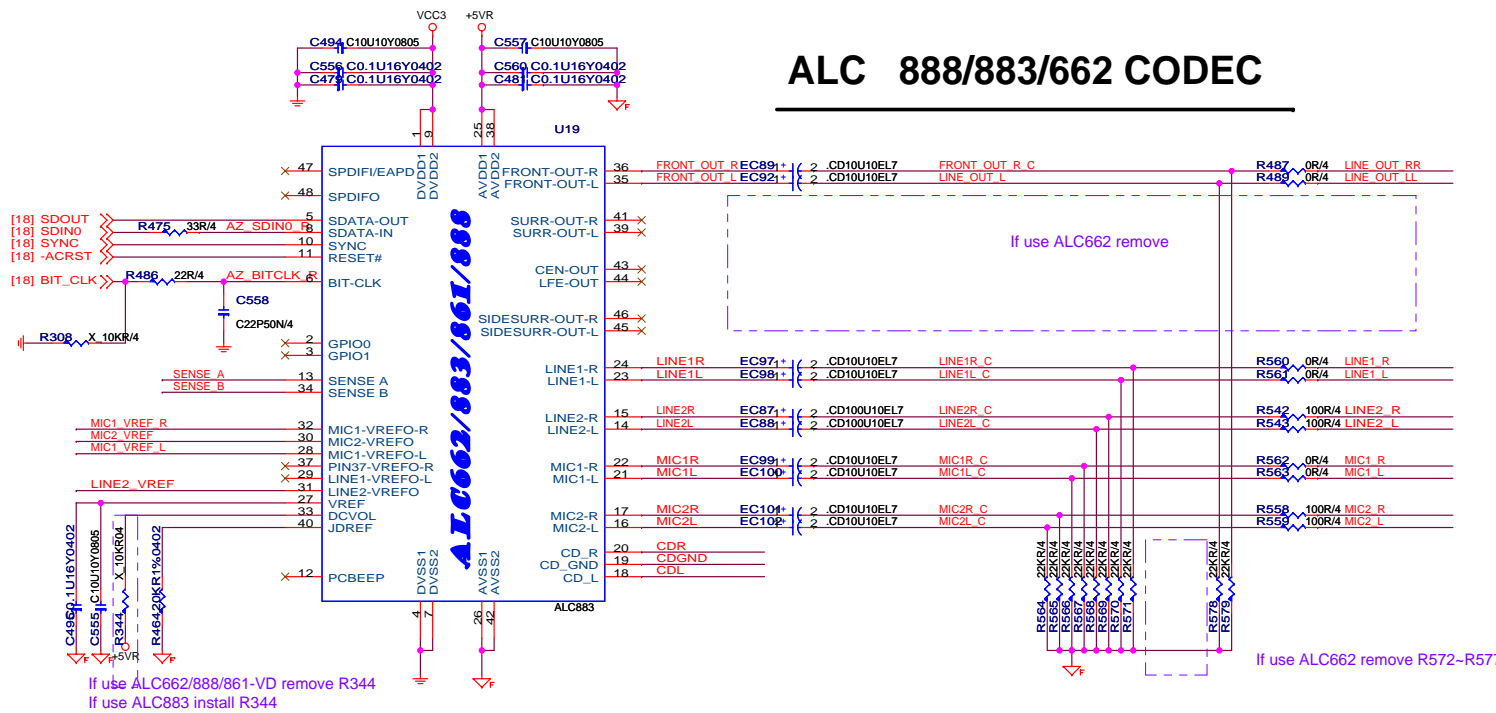


SOUTB	L:1K R466	PWMOUT 50%	FOR CPUFANOUT 1
	H:1K R465	PWMOUT100%	

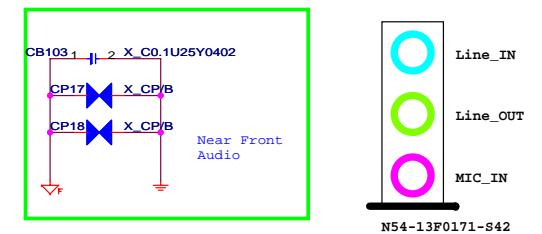
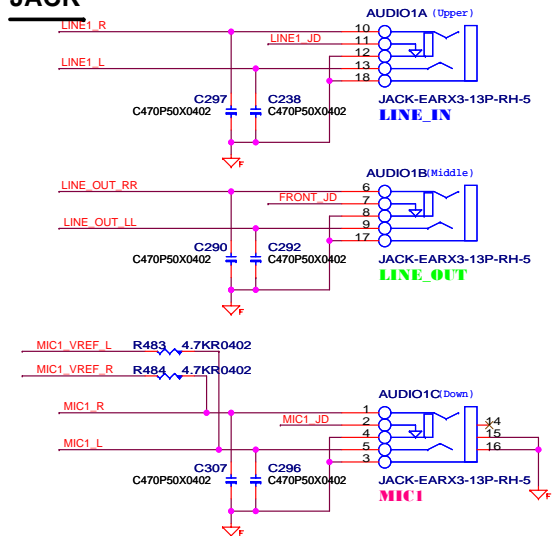
SOUTB	L:1K R466	24MHz	For CLKIN(pin 18)
	H:1K R465	48MHz	

Place Cap. as Close to
FWH < 350 mil

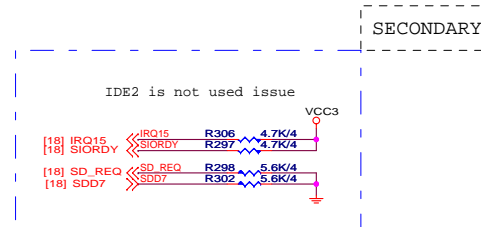
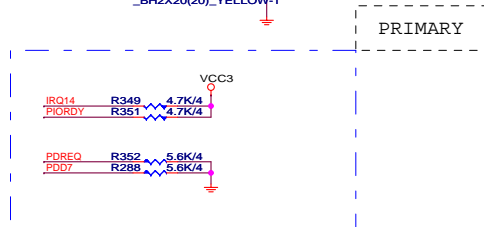
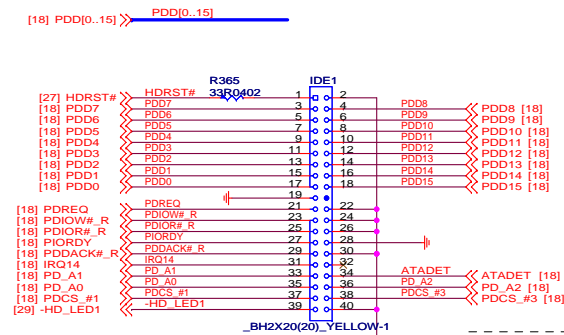
ALC 888/883/662 CODEC



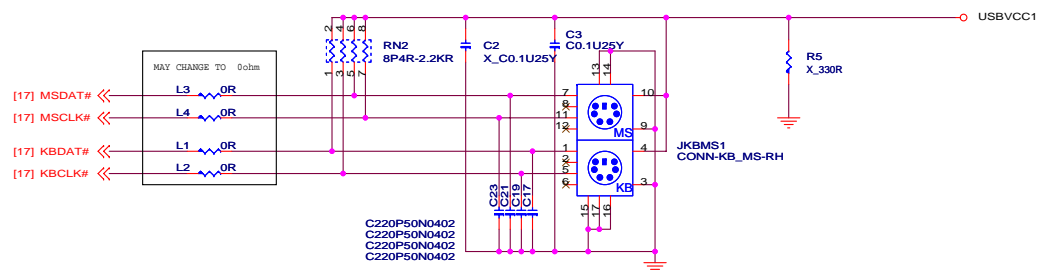
JACK



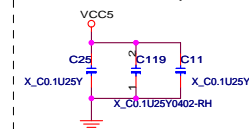
IDE1 AND IDE2



PS2 KB/MS

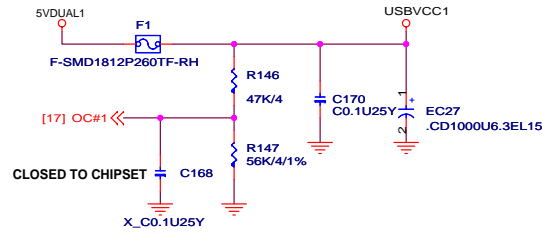


EMI

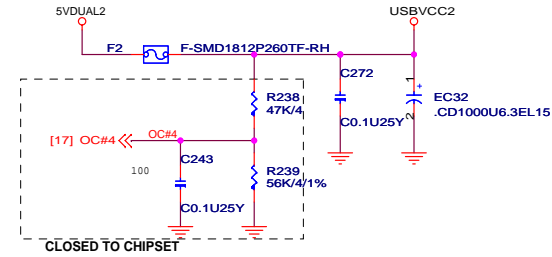


Rear USB Connectors

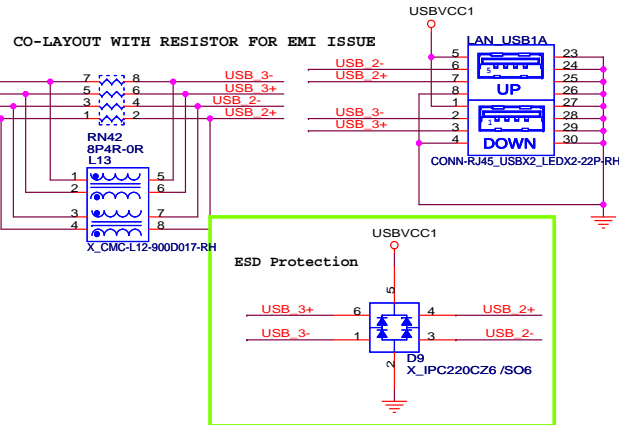
43m0BM X 2 A= 86mV



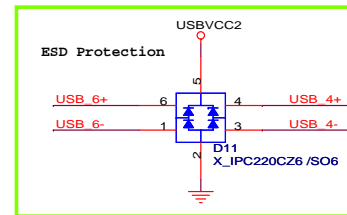
Front USB Connectors



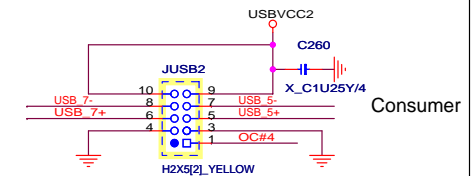
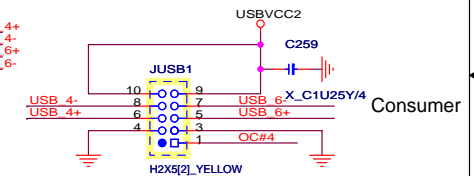
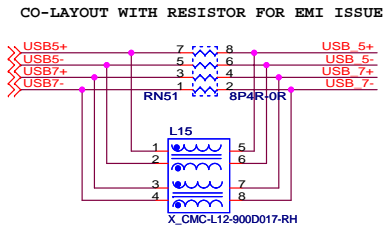
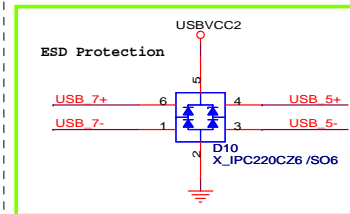
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



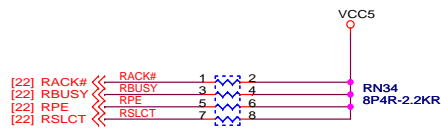
FRONT PANEL USB CONNECTOR FOR USB PORT 4,6



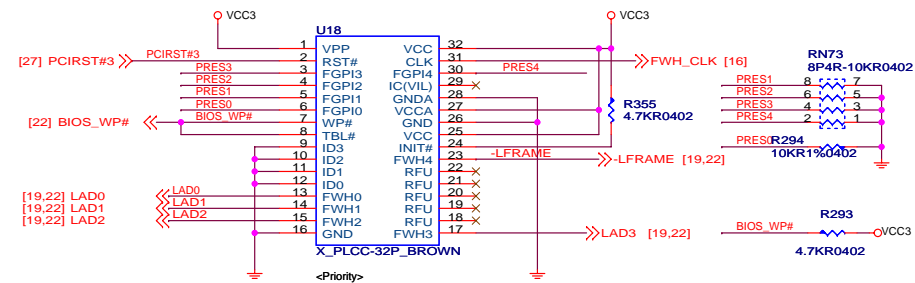
FRONT PANEL USB CONNECTOR FOR USB PORT 5,7



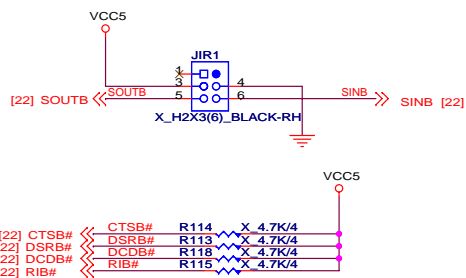
PRINTER PORT



Flash Rom

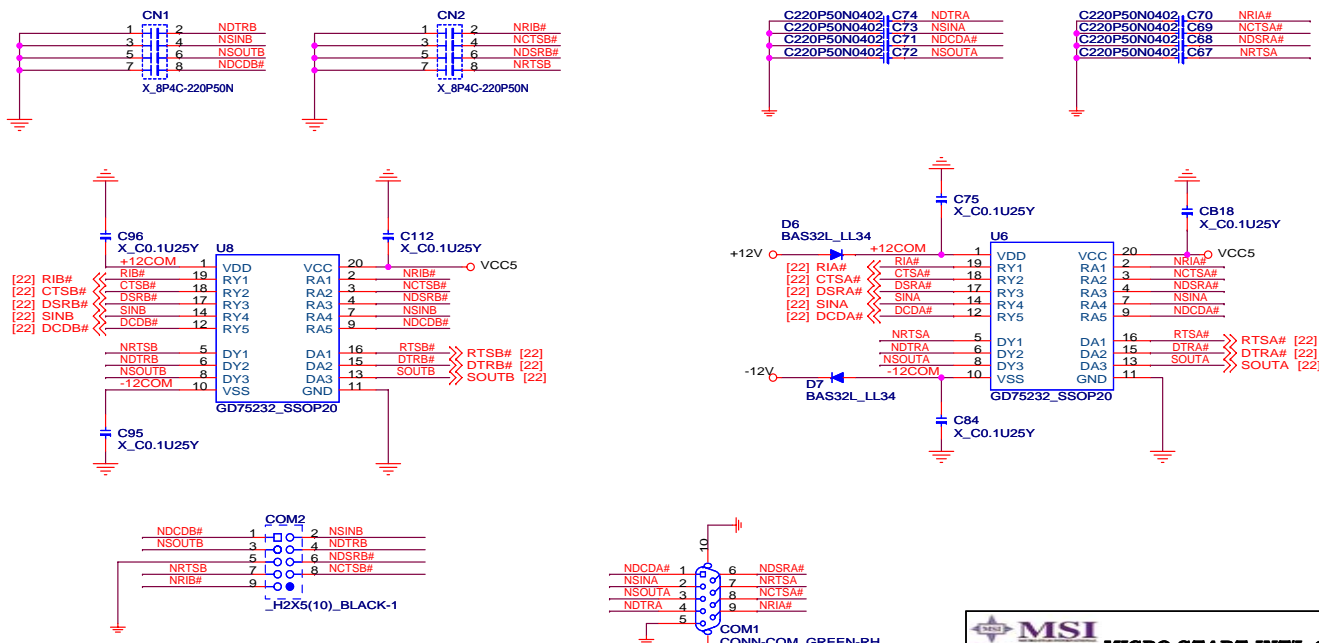


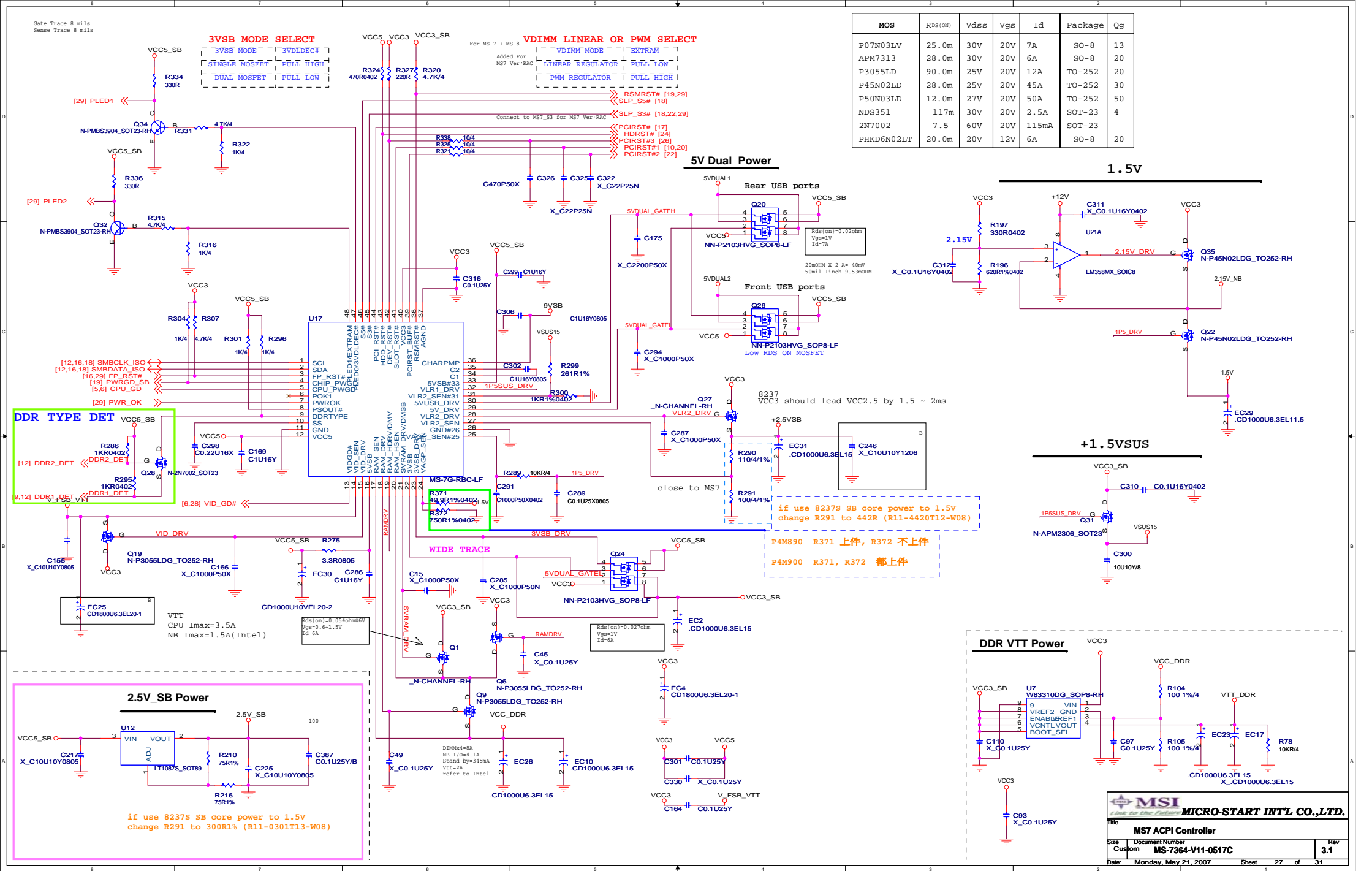
Intel Front IR Header



Notice: If system only get IR function but COMB. Those input pins need external pull up resistors incase transfer interrupt in IR.

SERIAL PORT 2





Pin19 & C547
through 2 VIAs
short Layer2
to Layer3

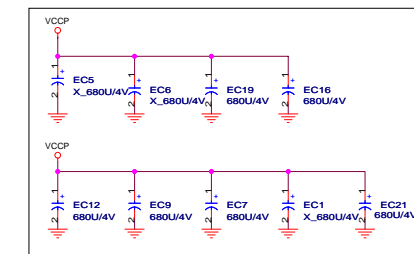


ST L6703 3PHASE FOR VR11

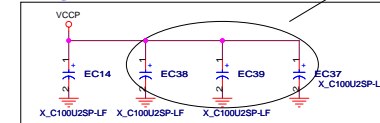
- Modify power solution.
1. R(40,41,38) change to 1.54K ohm.
 2. R23 change to 12.1K ohm.
 3. R54 change to 1.91K ohm.
 4. Remove EC8.
 5. R22 change to 137K ohm.
 6. C21 change to 100pf.
 7. C23 change to 10pf.

BOTTOM PAD
CONNECT TO GND
Through 9 VIAs

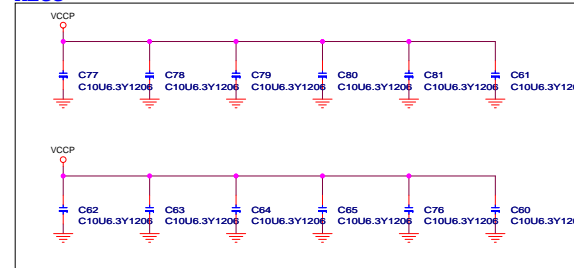
OS-CON



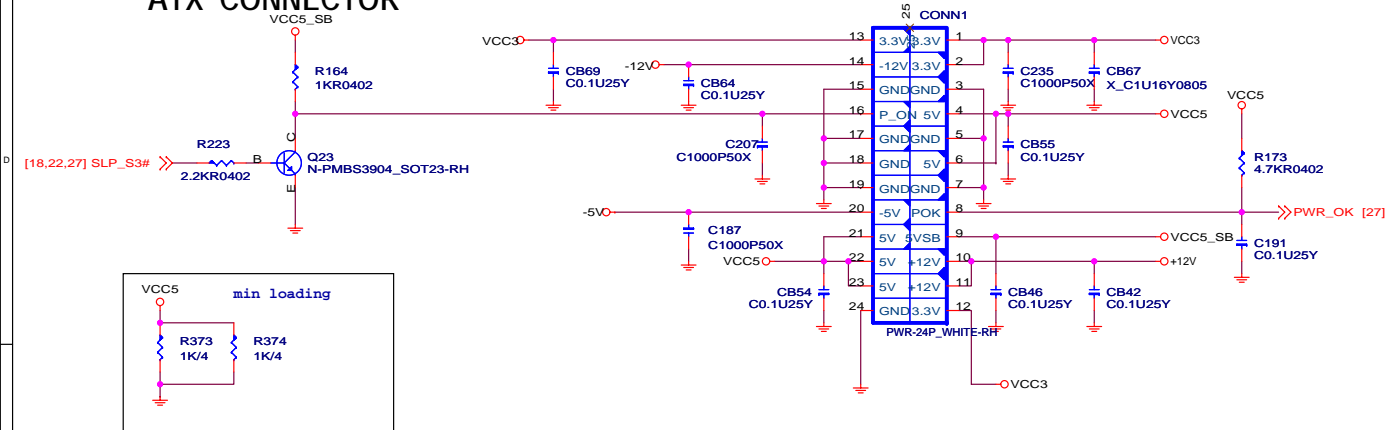
SP-CAP



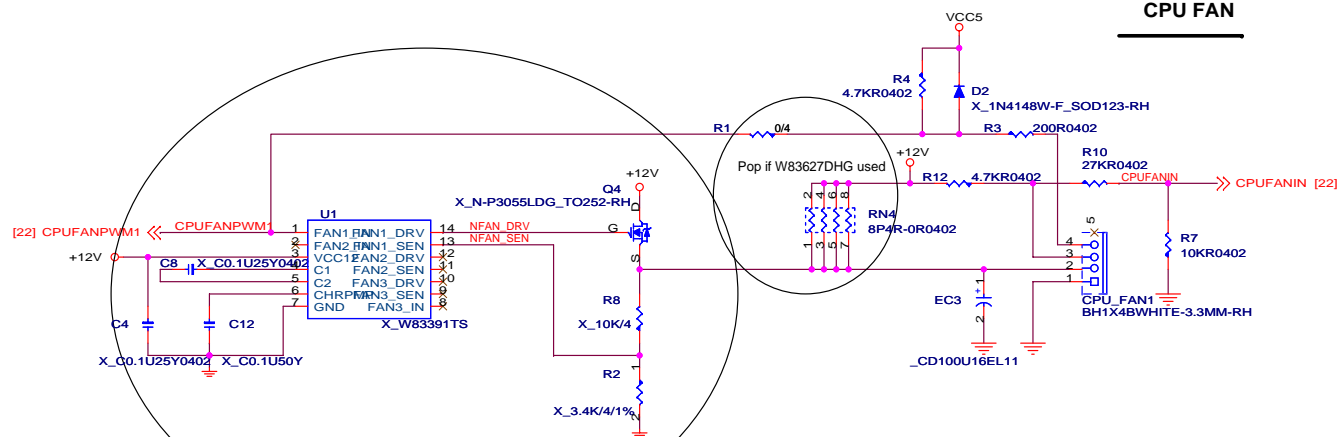
MLCC (Place into CPU Socket Cavity)



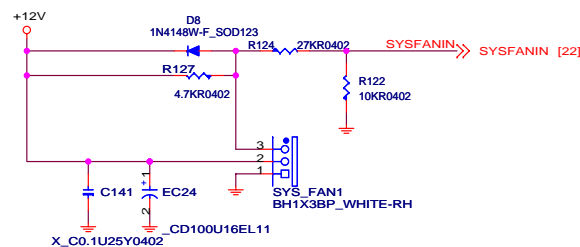
ATX CONNECTOR



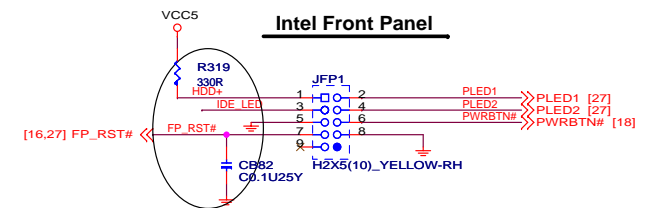
CPU FAN



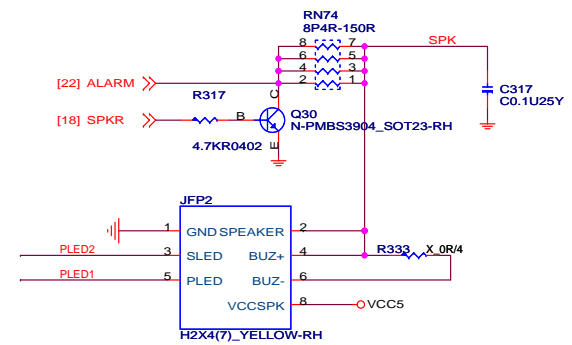
SYS FAN



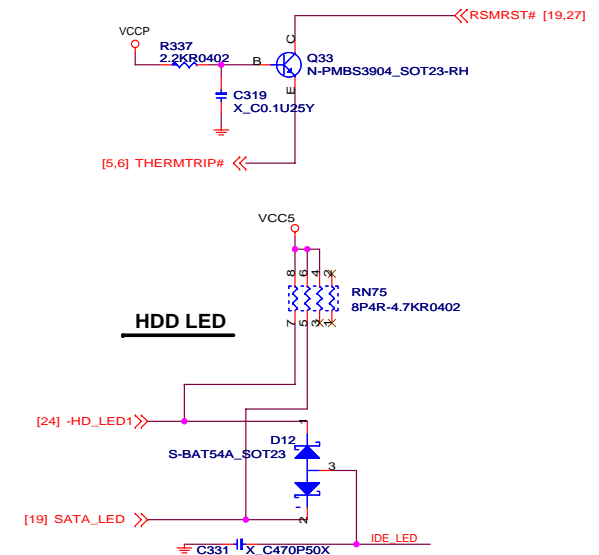
Intel Front Panel



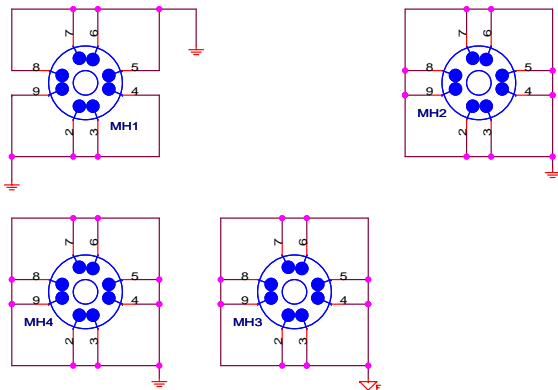
SPEAKER



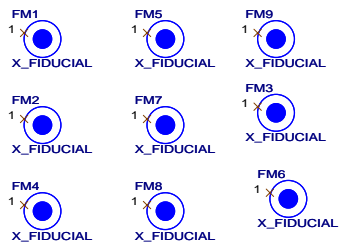
HDD LED



PCB OTHER COMPONENT

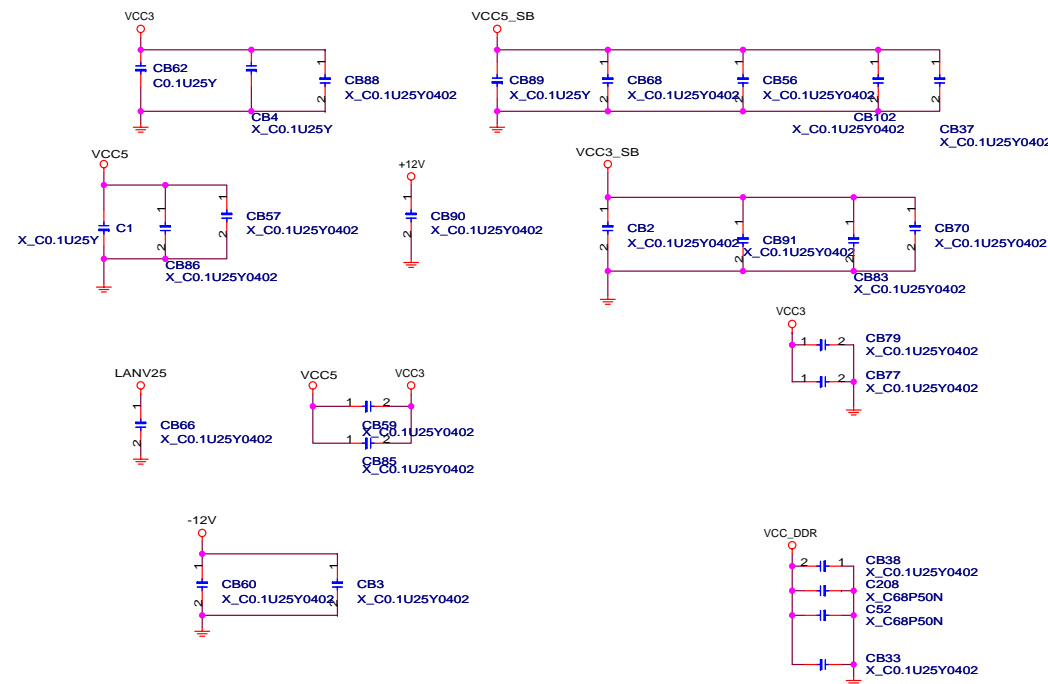


FIDUCIALS



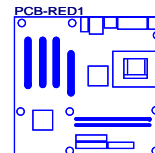
EMI

original EMI caps



Reserved EMI caps on 2006/10/31, from V3.0 to V3.1

Manual Part



PF0-0736412-E48

PF0-0736412-E48, 聯華
PF0-0736412-E55, 依頓



BAT1
BAT-BCR2032P-RH



BIOS1
PM49FL004T-33JCE-RH

MS-7364-V0A

- 1). the design circuit base on 7255
 - a. remove PCIE
 - b. change SIO to W8237EHG
 - c. change to 1080 (change CPU R impedance to 50& 49.9 to match 1080)
 - d. aupport DDRII & DDRI
 - e. only support one PCI slot
 - f. remove "Real USB" port (4 port -->2 port)
 - g. only support one IDE slot

MS-7364-V0B

- 1). add power team SOL :
 - a. EC8、EC18 to 680uF 4V , add EC7 680uF 4V
 - b. Modify C27 10P 、 R41 20Kohm 1% 0402
 - c. Cost down CHOKE (COIL1,COIL3,COIL4,) to L04-05A7201-W15

MS-7364-V0B (P4M890 Different With P4M900)

- A). NB CPUSLPIN (pin: AB32) need pull hiag ==> R167 pull high
- B). NB TESTIN (pin: AE35) need floating ==> remove R140
- C). NB main power 1.5Vchange to 1.6V
- C). NB 的 BOM 料

MS-7364-V10 (NB:P4M900/P4M890 SB:VT8237A/VT8237S)

- A). PM change NB, SB, SPEC , audio SPEC
- B). audio change to ALC883 co-lay 662
- C). remove USB 15KR to GND
- D). remove IDE damping R
- D). PIRQ#H pull high
- D). +2.5V Change TO 1.5V